In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1-9. (Cancelled)

10. (Original) A thin film transistor substrate, comprising at least:

a first stack structure and a second stack structure on the substrate, wherein the first stack structure comprises layers successively disposed which are a first conduction layer, a first insulation layer, and a semiconductor layer, and the second stack structure at least includes a second conduction layer;

an ohmic contact layer on a first region and a second region of the semiconductor layer, where the first region and the second region are disconnected;

a second insulation layer, positioned at least on the side surfaces of the first stack structure and the second stack structure and a part of the upper surface of the second stack structure;

a source electrode and a drain electrode, wherein the source electrode is positioned on a part of the second insulation layer and the ohmic contact layer in the first region, and the drain electrode is positioned on a part of the second insulation layer and the ohmic contact layer in the second region;

a passivation layer, positioned on the semiconductor layer, the source and the drain electrodes, and the second insulation layer; and

a transparent conduction layer, disposed on the passivation layer, wherein a first portion of the transparent conduction layer is electrically coupled to one of the source and the drain electrode and a second portion of the transparent conduction layer is electrically coupled to the second conduction layer of the second stack structure.

11. (Original) The substrate according to claim 10, wherein the second insulation layer is further deposited between the first stack structure and the second stack structure.

12. (Original) The substrate according to claim 10, wherein the first portion and the second portion of the transparent conduction layer is disconnected.

13. (Original) The substrate according to claim 10, wherein the first portion and the second portion of the transparent conduction layer is connected.

14. (Original) The substrate according to claim 10, wherein the first conduction layer and the second conduction layer are gate electrodes.

15. (Original) The substrate according to claim 10, wherein the transparent electrode layer is formed of indium-tin-oxide (ITO).

16. (Currently Amended) A thin film transistor substrate, comprising ~~at least~~:

a plurality of stack structures on the substrate, wherein each stack structure comprises layers successively disposed which are a first conduction layer, a first insulation layer, and a semiconductor layer;

an ohmic contact layer, positioned on a first region and a second region of the semiconductor layer, where the first region and the second region are disconnected;

a second insulation layer, positioned at least on side surfaces of the stack structures;

a source electrode and a drain electrode, wherein the source electrode is positioned at least on the ohmic contact layer in the first region, and the drain electrode is positioned at least on the ohmic contact layer in the second region, and wherein at least one of the source electrode and the drain electrode is positioned on a part of the second insulation layer;

a passivation layer, positioned on the semiconductor layer and the source and the drain electrodes; and

a transparent conduction layer, positioned on the passivation layer and electrically coupled to one of the source and the drain electrodes.

17. (Original) The substrate according to claim 16, wherein the second insulation layer is further deposited among the stack structures.

18. (Currently Amended) ~~The substrate according to claim 16,~~ A thin film transistor substrate, comprising:

a plurality of stack structures on the substrate, wherein each stack structure comprises layers successively disposed which are a first conduction layer, a first insulation layer, and a semiconductor layer;

an ohmic contact layer, positioned on a first region and a second region of the semiconductor layer, where the first region and the second region are disconnected;

a second insulation layer, positioned at least on side surfaces of the stack structures, wherein the second insulation layer is formed of silicon nitride;

a source electrode and a drain electrode, wherein the source electrode is positioned at least on the ohmic contact layer in the first region, and the drain electrode is positioned at least on the ohmic contact layer in the second region;

a passivation layer, positioned on the semiconductor layer and the source and the drain electrodes; and

a transparent conduction layer, positioned on the passivation layer and electrically coupled to one of the source and the drain electrodes.

19. (Original) The substrate according to claim 16, wherein the first conduction layer is a gate electrode.

20. (Original) The substrate according to claim 16, wherein the transparent electrode layer is formed of indium-tin-oxide.

21. (New) The substrate according to claim 16, wherein the passivation layer is further positioned on the second insulation layer.

22. (New) The substrate according to claim 16, wherein the second insulation layer is formed of silicon nitride.

23. (New) The substrate according to claim 18, wherein the second insulation layer is further deposited among the stack structures

24. (New) The substrate according to claim 18, wherein the first conduction layer is a gate electrode.

25. (New) The substrate according to claim 18, wherein the transparent electrode layer is formed of indium-tin-oxide.

26. (New) The substrate according to claim 18, wherein the passivation layer is further positioned on the second insulation layer.